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Hardware/Software Technologies for High-Performance Systems TIC2002-00750

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Abstract

The aim of this project is the development of technologies to enhance the performance of computing systems through the combined use of hardware and software strategies. The project is composed of a set of interacting research lines that can be classified in two main areas: architecture and design of hardware components, on the one hand, and algorithm tuning on new computing platforms, on the other.

With regard to the first area, the project explores different approaches to improve the cost-performance-power tradeoffs in the conception of both general purpose processors, and special-purpose systems, with special attention to the embedded systems domain. The improvement of design methodologies to generate special purpose hardware, when needed, is also considered.

In the area of algorithm-platform tuning, the goal is the development of algorithms and methodologies that efficiently exploit the computational resources of current computing platforms. We focus on the development of new algorithms that exploit locality along the different levels of the computing system. We intend to export the results of this research into software libraries that include the proposed optimizations and to validate them on high challenge applications over several fields of interest.

From the methodological point of view, this project is organized in four main research lines, as follows: a) algorithms, architectures, and applications, b) processors and optimization, c) embedded systems design, and d) asynchronous systems.

Keywords: Supercomputing, Parallel Computing, Parallel Numerical Algorithms, Advanced Microarchitecture, Architectures for Embedded Systems, Dynamic optimization, Architectural Level Synthesis, Reconfigurable Computing, Power-aware architecture, Computer Graphics, Asynchronous Systems.

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1 Project goals

This report is organized according to the four main research lines that were defined in the initial project proposal. The specific goals of each research line are summarized in this section, while Section 2 is devoted to describe the main achievements reached since the beginning of the project (December 2002).

1.1 Algorithms, architectures, and applications

a) Optimization of multilevel applications on current microprocessors. The goal of this module is the optimization of the different multilevel algorithms tackled in this project in high-end microprocessors. As multilevel algorithm we understand algorithms where the information is processed using different levels of detail. Well-known examples are the discrete-wavelet transform (DWT) and multigrid-based solvers (MG). Most research about this topic has been concentrated on cache-aware implementations, i.e. alternative ways to perform the computations attempting to more efficiently exploit more efficiently the memory hierarchy. This module builds on these efforts and try to improve them focusing on small-scale SIMD. Our long-term goal is to transfer the results of this research into software libraries, which should provide tuned versions of the main components of target applications, and apply them to relevant applications.

b) Parallelization of multilevel applications. This module constitutes a natural extension of the previous one. It addresses high-challenge multilevel applications in which execution time should be reduced even further. In our original proposal, we planned to achieve these speedups using message-passing and low-cost PC clusters as computing platform. However, as a result of the widespread adoption of architectures with additional levels of parallelism (e.g. Simultaneous Multithreading and Multiprocessor on Chip are presented in most high-end microprocessors) we have opted to change our focus toward Thread Level Parallelization (TLP).

c) Optimization of 3D-visualization applications. The main aim of this part is the implementation of a terrain generator and a real-time terrain 3D-viewer. The objectives of this module are the following: fast terrain-data access, efficient data storage, adaptive triangulation, multiresolution visualization, high geometric rendering performance.

1.2 Processors and optimization.

Within this line, the project is focused on the study and implementation of power-efficient techniques, with special emphasis in low power design and dynamic optimization.

a) Low power design. This module considers main sources of power consumption in general-purpose high-performance and embedded processors. The goal is the development of techniques for lowering the power consumption without significant penalty in performance. These techniques can be divided into the following two categories:

- Adaptive low-power techniques, which exploit application variability to save energy. Their target hardware includes branch and value predictors, instruction window, load-store queue, and fetch engine.
- Software techniques, which enable finding power/performance trade-offs. The focus is mainly placed on efficiently exploiting the available hardware for each application. Compiler support is usually required.

b) Dynamic optimization. The goal of this module is the study of the optimization of programs during execution by means of a mixture of hardware and software. Optimization of program execution can take advantage from the cooperation of hardware and software mechanisms so that part of the analysis and optimizations traditionally performed by hardware can be executed by software. It also involves a reduction in power consumption. Information about the program being executed must be collected on-the-fly and given to a Virtual Machine Monitor that will use it to optimize the program while it is being executed. These techniques are particularly useful for Java Virtual Machines.

1.3 Embedded systems design

a) Synthesis of application specific circuits with independence of the descriptive style. The overall goal of this module is to investigate on high-level methodologies and algorithms able to obtain digital designs with a quality level irrespective of the way the specifications are written. The research is based on previous studies on how behavioural specifications are interpreted by synthesis tools, and which are the main aspects that influence the quality of the results. These aspects are basically related to data types and primitive operators used in the specification, as well as, the language constructs used by the designer. This research pursues:

- The development of a set of new algorithms for the scheduling and allocation of behavioural descriptions not affected by the above mentioned aspects.
- The development of code-to-code transformation algorithms able to adapt designer friendly specifications into other equivalent ones, more suitable to be synthesised by conventional design tools.

b) Tuning of application specific processors. This module tries to research on methodologies that allow the embedded system designer to tune its designs to certain application, running environment, or performance/area/power requirements. Due to its intrinsic relevance, and the experience of the foreign research teams we collaborate with, the particular domain selected is the tuning of memory subsystems of embedded multimedia systems.

c) Reconfigurable computing. The aim of this module is the efficient management of the information transfers between the external memory and the on-chip internal memories of a coarse-grained dynamically reconfigurable processor. These transfers concern not only data to be processed, but also the contexts that personalize the functionality of the configurable processor. Therefore, an intelligent management of these movements should lead to better execution times, and lower power budgets. Additionally, our goal is to study the main factors that are responsible for the inefficiency of the target reconfigurable processor architecture (i.e. MorphoSys, developed in the University of California at Irvine) and, as a consequence, to propose improvements in the architecture.

1.4 Asynchronous circuits

a) CAD tools and methodologies. The goal of this module is to find a design methodology, and to develop CAD tools, that allow increasing productivity in the design of complex asynchronous circuits. With this intention, the proposed methodology attempts to exploit the design flow of commercial CAD tools developed for synchronous design.

b) Asynchronous pipelines. This module is devoted to study the behaviour of asynchronous pipelines and to establish the techniques that allow increasing their performance. Specifically, the

influence of the variable latency of the stages and the input patterns in the global performance of the pipeline are studied in this module.

2 Level of success reached in the project

At the time of writing this report, the project has consumed 22 months out of its three-year schedule. However most of the proposed goals and tasks have already been accomplished. This section summarizes the main scientific achievements reached till now, following the same structure of the previous section.

2.1 Algorithms, architectures, and applications

a) Optimization of multilevel applications on current microprocessors. We have introduced a novel scheme to structure the computation of the wavelet transform that enables an efficient exploitation of both the memory hierarchy and small scale SIMD parallelization. The proposed scheme does not depend on the particular filter employed and can be implemented in most platforms [CTPP03a] [CTPP03b]. Based on this scheme, we have developed a software library that provides various lifting-based wavelet transforms. Currently, we are integrating this library into a reference implementation of the JPEG2000 image coding standard. This integration will improve the diffusion and understanding of our results and to facilitate further comparisons. Finally, we should remark that we have also demonstrated that small scale SIMD extensions can be beneficial not only for multimedia programs, but also for numerical codes such as Multigrid [GLPP03a] [GLPP03b].

b) Parallelization of multilevel applications. Apart from the parallelization of a Multigrid-based Navier-Stokes solver [PMLT03], the activities of this module have been concentrated on the DWT. Using as test-beds the codes developed in 2.1a we have proposed different strategies to parallelize this transform on Simultaneous Multithreading Architectures (SMT) and General Purpose Graphics Hardware (GPUs) [TLPT04a]. Focusing on SMT architectures, unlike most traditional SMPs, parallelization strategies based on functional partitioning (FP) can outperform traditional Data-Partitioning counterparts (DP). Competition among threads for memory bandwidth and data cache works against the DP strategy for large input datasets. [TGPP04]

c) Optimization of 3D-visualization applications. Terrain rendering is an expensive computational task when high resolution and big terrains are required. One possible optimization is the view-dependent LOD (level of detail) simplification, where areas near the point of view demand more detail than those areas that are far away. We have developed a new algorithm for irregular terrains, denoted as QuadTIN (Quadtree-based Triangulated Irregular Network), that achieves real-time visualization by traversing a quadtree hierarchy in order to select the vertices required for a given resolution. The experimental results have shown that is possible to render a terrain of two million points at 50 frames per second with an error tolerance of one pixel on a screen of 1024x 768 pixels [LPT03].

2.2 Processors and optimization.

a) Low power design. We have shown that by exploiting program behaviour repetition, we can implement branch predictors customized to particular program needs. This customization results in minimal degradation of prediction accuracy and performance, while achieving notable energy savings [CPPT03a, CPPT03b, HCPP03]. In addition, we are considering exploiting program behaviour repetition to optimize other aspects of system design. In particular, we have already

undertaken the study of the same approach for the load-store queue and the trace cache. We are also looking at using other high-level program information to optimize resource allocation at the microarchitecture level to improve energy efficiency.

In embedded system context, our research has been focussed on the efficient exploitation of the memory hierarchy since it represents the major source of power consumption and the main performance bottleneck. Within this scope, we have developed a technique for integrated task-scheduling and data assignment, which guarantees a trade-off between power and performance in dynamic applications [MGBB03, MGBB04]. In order to further optimize the available memory bandwidth we have also developed a loop fusion technique that overcomes the traditional conformability limits [MGPC04a, MGPC04b].

b) Dynamic optimization. In order to study the effect of dynamic optimization in system performance we have developed an experimental environment based on the Java Research Virtual Machine called Jikes, which has been developed by IBM T.J. Watson Research Centre. We used it to measure performance degradation due to garbage collection, because the automatic memory management is one of the main causes of overhead. We proposed a new adaptive garbage collection mechanism, which improves performance of the system. [VOOT03a] [VOOT03b] [VOOT04] [VOT04a] [VOT04b]. We are also beginning to study the effect of garbage collection on power consumption and real-time response of embedded systems in order to characterize their design space. This knowledge will help the automatic design of multimedia embedded platforms. [VACT04].

2.3 Embedded systems design

a) Synthesis of application specific circuits with independence of the descriptive style. The preliminary research on this topic clearly showed that the designer's coding style has a strong impact on the quality of the synthesised circuits. Among the issues related with coding style, we identified two specific factors that have a very important influence on the quality of the synthesis process: the use of heterogeneous data representations, and code variability derived from the use of the control flow sentences provided by the specification language. This research is producing a collection of new algorithms aimed at reducing the impact of these two factors by means of new allocation and scheduling algorithms, able to efficiently synthesise circuits with multiple data formats [MMH03a] [MMH03b] [MMH03c] [MRMH04a], as well as new strategies for pre-synthesis code transformations [Peña04].

b) Tuning of application specific processors. Within the framework of the research domain chosen in this module, that is, the tuning of memory subsystem of multimedia embedded systems, a complete methodology for the efficient management of the dynamic memory (portion of the memory allocated and released in run-time) has been proposed [AMCM04a]. This methodology face up the problem from three different points of view, taking into account different sets of design constraints. From the software side, the methodology proposes a set of source code transformations that enable the designer to select the best data representations of the data types present in multimedia applications [LAYF03] [LACD03] [ALMF03] [LAMC03] [ALCD04]. From the operating system side, the methodology defines a structured design flow for developing application specific (or custom) dynamic memory managers [AMLF03] [AMPC04a] [AMCM04b] [AMCM04c] [AMPM04] [LAYC04]. Finally, from the hardware side, some physical memory architecture-aware techniques for dynamic data allocation have been studied [PMAB04].

In the context of application specific processors, the analysis and development of flexible peripherals interfaces have been also studied. Our results show that dedicated yet flexible peripherals for high-speed serial interconnects can be implemented using existing network processor building blocks, thus avoiding inflexible ASIC blocks [SGGW04] [SGGK03].

c) Reconfigurable computing. It has been met the goal to get an efficient management of the information transfers from/to the external memory and the on- chip internal memories of a coarse-grained dynamically reconfigurable processor, maintaining in the internal memories the most frequently used data. This scheduling has taken into account the existence of an on-chip memory hierarchy that in previous approaches had not been considered, and has detected the shared data among different tasks of DSP and multimedia applications, in order to be candidates to be maintained in the on-chip memories. Thus, we have got substantial savings in execution times and energy consumption [SFAD03]. We also developed the initial steps of a dynamic data management system, in order to be used with interactive applications that are foreseen as the new workloads of the coarse-grained reconfigurable architectures [SDTL03] [RSFH04].

2.4 Asynchronous circuits

We have proposed a high-performance GALS architecture that incorporates an aggressive asynchronous technique that we call Data Classification based on Data Latency (DCDL). The key idea behind this technique is to classify input data into several classes depending on the delay required for their computation and to capture computed data after such delay.

a) CAD tools and methodologies. In order to be able to classify input data, it is needed to know the delay of the functional units for the different classes of input vectors. It is also vital to know how the classification of input vector is influenced by the way the FU is described and synthesized; and to deduce rules that allows obtaining optimal implementations under the selected GALS approach, but using commercial –that is, synchronous flavour– tools. Currently we have finished the study of the behaviour of data on different types of adders, and we are studying the influence of the synthesis constraints in the classification of the data [CGHL03] [CGHL04].

b) Asynchronous pipelines. In order to check the improvement of the processor's performance, when the processor is implemented using the previously stated approach, we are developing an event-driven simulator of GALS architectures. Previously, we have defined and validated, using Petri Nets, the asynchronous communication protocol which synchronizes the different clock domains. To assure the validity of this communication mechanism we have modelled the protocol using Signal Transitions Graph (STG) and checked it using Petrify [LGHL03]. The potential to improve the processor performance, when this communication protocol is used, has been explored by describing -at RTL level- and implementing a GALS DLX-like processor, in which we have applied our communication protocol and the DCDL technique.

3 Result indicators

3.1 Publications

The list of publications that derived form this project is in clear concordance with the plan for dissemination of results that was described in the initial proposal. It should be highlighted that this research has already produced results that have been published in the journals and conferences that were listed in the proposal as the most prestigious of the field. This includes IEEE Micro, IEEE

Design & Test of Computers, ACM Trans. on Design Automation of Electronic Systems, Integration, Parallel Computing, IEEE Trans. on VLSI Systems … among the journals, and DATE, DAC, FPL, ISSS, ISPLED, VECPAR, IPDPS, PDP … among the conferences.

In summary, during the first two years, the project produced:

- 21 publications in journals listed in JCR (marked with * in the references)
- 33 papers in international conferences
- 11 papers in national conferences
- 1 book chapter

The full list of publications is included in section 4.

3.2 Ph. D. Thesis

Luis Piñuel Moreno, "Ejecución especulativa basada en predicción de valores", Universidad Complutense, 2003

Olga Peñalba Rodríguez, "Optimización del uso compartido de recursos durante la síntesis conductual de sistemas con modelo de ejecución condicional", Universidad Complutense, 2004

Marcos Sánchez-Élez Martín, "Gestión de la planificación de datos en sistemas reconfigurables multi-contexto orientada a baja energía", Universidad Complutense, 2004 (presentation date: November 5, 2004)

Juan Carlos Fabero Jiménez, "Métodos numéricos sobre teselado hexagonal para la simulación de ecuaciones en derivadas parciales ", Universidad Complutense, 2004, (pending of defining the Ph.D. presentation date).

Additionally, the ongoing research of Ph.D. candidates working in the project should produce four more Ph.D. thesis before the end of the project (December 2005).

3.3 Cooperation with other groups

Most of the research described in section 2.3.b, as well as, some tasks of the work described in sections 2.1.a, 2.2.a, and 2.2.b are being carried out in cooperation with the "Dipartimento di Elettronica, Informatica e Sistemistica de la Università degli studi di Bologna" (Italy) and the division of "Design Technology for Integrated Information and Telecom Systems (DESICS)" of the Inter-university Micro-Electronics Center (IMEC)" of Leuven, Belgium. This cooperation is being implemented through a series of stays of researchers of the project at IMEC, and several visits of IMEC staff to UCM. As a fruit of these relationships, IMEC and UCM have recently signed a specific agreement for scientific and technological cooperation.

The research described in section 2.2.a is also developed in cooperation with the Department of Electrical and Computing Engineering of the University of Rochester, NY, USA, where three of our researchers have done stays in the last year.

The cooperation of our group with the Department of Electrical and Computer Engineering of the University of California at Irvine, in the field of reconfigurable computing (section 2.3.c), started more than five years ago. In this project the group of Prof. Nader Bagherzadeh has been closely involved to the point that he is serving as co-director of the Ph.D. thesis of one of the young researchers of our group.

The research about flexible peripherals interfaces (section 2.3b) has been carried out within the MESCAL project, and under the advice of Prof. Kurt Keutzer from the Department of Electrical Engineering and Computer Science of the University of Berkeley

As can be seen in section 4, all this cooperation with prestigious research groups from abroad is producing joint publications in journals and top-level conferences.

3.4 Trained personnel

In addition to the researchers who have a contract with UCM and are (or have been) working towards their Ph.D., this project included three additional persons who have a grant specifically provided by the project. This leads to a total amount of eleven persons receiving research training, with at least eight of them having a clear chance to defend their Ph.D. thesis before the end of the project.

3.5 Participation in European projects

The group is participating in the European Network of Excellence on High-Performance Embedded Architectures and Compilers (HiPEAC), Project No.: IST-004408. The official starting date of this network is September 1, 2004.

3.6 Technology transfer activities

Starting January 2004 the research group has a contact with CASANDRA Energy Systems to provide consulting services (code optimization), and computational support in the development and exploitation of predictive models of energy production in wind farms.

The research group is also involved in PCM (Parque Científico de Madrid) as a horizontal computational node of INB (Instituto Nacional de Bioinformática) funded by Genoma España.

4 References

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